Active Matching with Common-Gate MESFET's

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Abstract — **The electrical performance of the common-gate MESFET input stage across multi-octave frequency bands has been analyzed. Based on the device's common-source parameters, formulas for the circuit's admittance and noise parameters have been derived that allow one to calculate its gain, reflection coefficients, and noise figure. The influence of the circuit elements on the input stage's performance, especially on the noise figure, are studied. Finally, the electrical behavior of a two-stage unit consisting of a common-gate input stage followed by a common-source amplifier stage is discussed.**

I. Introduction

THE COMMON-GATE FET employing series inductive feedback is widely used in oscillator design. Its capability to induce negative resistance conditions at one or both of its ports, however, is only one important characteristic of the MESFET in common-gate configuration. Another outstanding feature that has attracted the attention of solid-state amplifier designers is the circuit's excellent input match over wide frequency bands. The latter of these two characteristics, i.e., active matching, is the subject of this paper.

The feasibility of the common-gate input stage as an active matching device at microwave frequencies has been demonstrated by a number of researchers, and experimental results have been reported in the literature [1]–[3]. While design efforts have mostly been expended at frequencies $f < 5$ GHz, where biasing and stability pose less of a problem [1], [2], W. C. Peterson *et al.* [3] have demonstrated $G = 7.2 \pm 1.2$ dB of small-signal gain in a four-stage monolithic amplifier from 0.7 GHz to 9.0 GHz. The unit's input VSWR was better than 2:1 between 0.1 GHz and 12 GHz. It is the primary purpose of this paper to analyze the theoretical performance of the common-gate FET input stage at microwave frequencies and to develop analytic expressions that aid in the understanding of such circuits. Special emphasis is focused on wide-band applications, which make it mandatory to include the second stage into the analysis for it presents a complex set of load impedances to the input network that has a profound impact on the amplifier's overall performance. In addition, the second stage provides most of the two-stage unit's gain, making it a significant factor in the composition of the overall noise figure.

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II. The Signal and Noise Parameters

A. The Current Matrix

GaAs MESFET's, when used in amplifiers, are almost exclusively operated in a common-source configuration. Since the characterization of the transistors is also performed and their S-parameters, with a few exceptions, are published for the grounded source device, we base our analysis on common-source parameters. The circuit of the common-gate input stage in its general form is shown in Fig. 1. The series impedance Z_s, the parallel admittance Y_P, and the gate and drain admittances Y_G and Y_D have been added to the circuitry to increase the stability, shape the gain, and improve the output match. As will be shown later, not all of these elements are necessary or even desirable for the circuit's performance for they may impair its noise figure. The analysis, though employing elementary algebra, is rather involved. Hence, to make matters less complicated, we divide the treatment into two steps by first analyzing the inner circuit of Fig. 1 and then adding the remaining elements (Y_P, Y_G, and Y_D), i.e., the outer circuit. Conducting the analysis by means of the Y-parameters and the equivalent noise parameters (R_n, G_n, and Y_{cor}) [4] in accordance with Fig. 2(a) and (b) adds further to the convenience of the mathematical procedure.

1) The Inner Circuit: Once the Y-parameters and the noise parameters of the common source FET (Fig. 2(a) and (b)) are known, we are able to determine those of the subcircuit of Fig. 2(c), which is identical to the inner circuit of Fig. 1 and equivalent to that of Fig. 3. The latter is more detailed and includes the noise sources of the MESFET and that of the series impedance. Application of Kirchhoff's rules to the circuit of Fig. 3 leads us to the signal and noise currents at the terminals of the common-gate MESFET employing series feedback. Expressed in matrix representation, they are

$$\begin{bmatrix} I_1^I \\ I_2^I \end{bmatrix} = \underbrace{\begin{bmatrix} Y_{11}^I & Y_{12}^I \\ Y_{21}^I & Y_{22}^I \end{bmatrix}}_{\text{Signal Matrix}} \begin{bmatrix} V_1^I \\ V_2^I \end{bmatrix} + \frac{1}{1+Z_sY_{11}} \cdot \underbrace{\begin{bmatrix} (Y_{21}+Y_{11}) & (1-Z_sY_{21}) \\ -Y_{21} & Z_sY_{21} \end{bmatrix}}_{\text{Noise Matrix}} \begin{bmatrix} (v_1+v_s) \\ -i_1 \end{bmatrix} \quad (1)$$

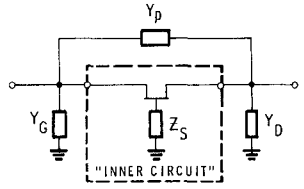


Fig. 1. Schematic of the common-gate input stage.

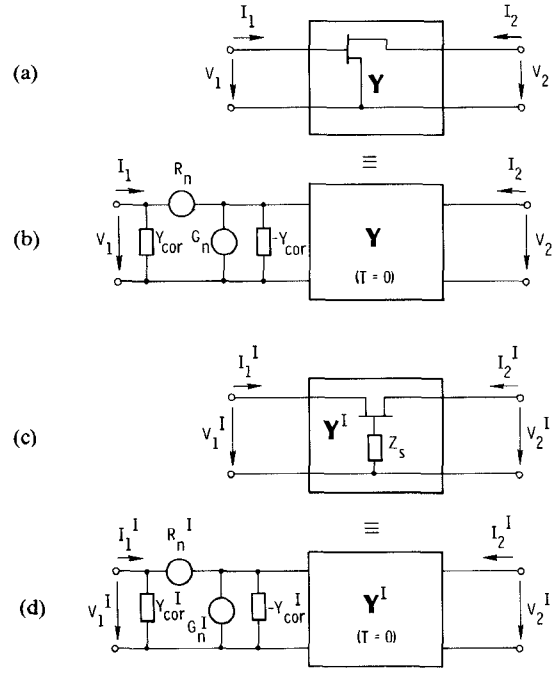


Fig. 2. Conversion of the device's common-source parameters ((a) admittance and (b) noise) into its common-gate parameters ((c) admittance and (d) noise) when applying series feedback.

where

$$Y_{11}^{I} = \frac{1}{1+Y_{11}Z_s} \cdot \left[(Y_{11}+Y_{12}+Y_{21}+Y_{22})+Z_s(Y_{11}Y_{22}-Y_{12}Y_{21})\right] \tag{1a}$$

$$Y_{12}^{I} = \frac{-1}{1+Y_{11}Z_s}\left[(Y_{22}+Y_{12})+Z_s(Y_{11}Y_{22}-Y_{12}Y_{21})\right] \tag{1b}$$

$$Y_{21}^{I} = \frac{-1}{1+Y_{11}Z_s}\left[(Y_{22}+Y_{21})+Z_s(Y_{11}Y_{22}-Y_{12}Y_{21})\right] \tag{1c}$$

$$Y_{22}^{I} = \frac{1}{1+Y_{11}Z_s}\left[Y_{22}+Z_s(Y_{11}Y_{22}-Y_{12}Y_{21})\right] \tag{1d}$$

are the parameters of the signal matrix. The superscripts $(\ )^{I}$ and $(\ )^{II}$ distinguish between the parameters of the inner circuit $(\ )^{I}$ and those of the common-gate input stage $(\ )^{II}$ shown in Fig. 1.

The Y-parameters of the signal matrix may be significantly simplified if the condition

$$Y_{22} \gg Z_s(Y_{11}Y_{22}-Y_{12}Y_{21}) \tag{2}$$

is satisfied for both the real and the imaginary part. In this case

$$Y_{11}^{I} \cong \frac{1}{1+Y_{11}Z_s}(Y_{11}+Y_{12}+Y_{21}+Y_{22}) \tag{3a}$$

$$Y_{12}^{I} \cong \frac{-1}{1+Y_{11}Z_s}(Y_{22}+Y_{12}) \tag{3b}$$

$$Y_{21}^{I} \cong \frac{-1}{1+Y_{11}Z_s}(Y_{22}+Y_{21}) \tag{3c}$$

$$Y_{22}^{I} \cong \frac{1}{1+Y_{11}Z_s}Y_{22}. \tag{3d}$$

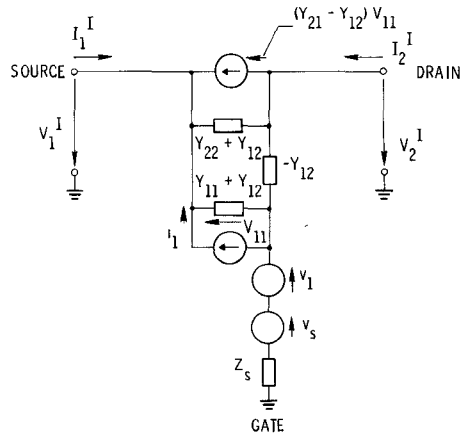


Fig. 3. Equivalent two-port of the common-gate MESFET with series feedback (inner circuit).

Meeting the requirements of (2) obviously depends on the transistor's characteristics and the series impedance Z_s. For example, in the case of the device represented by the equivalent circuit of Fig. 4, the approximation formulas (3) may be used for frequencies $f \leqslant 10$ GHz as long as a resistor $R_s \leqslant 10\ \Omega$ serves as the series feedback impedance Z_s. The element values tabulated in Fig. 4 have been obtained by matching the S-parameters of the equivalent circuit with those measured on a GaAs MESFET with a 0.5×300-μm gate and a 2×10^{17}-cm^{-3} carrier concentration.

2) The Common-Gate Input Stage: Derivation of the currents for the entire circuit of Fig. 1 can be easily accomplished by superposition of the currents in accordance with Fig. 5. Hence, the total currents are

$$\begin{bmatrix} I_1^{II} \\ I_2^{II} \end{bmatrix} = \underbrace{\begin{bmatrix} (Y_{11}^{I}+Y_G+Y_P) & (Y_{12}^{I}-Y_P) \\ (Y_{21}^{I}-Y_P) & (Y_{22}^{I}+Y_D+Y_P) \end{bmatrix}}_{\text{Signal Matrix}} \begin{bmatrix} V_1^{II} \\ V_2^{II} \end{bmatrix}$$

$$+ \underbrace{\frac{1}{1+Z_sY_{11}}\begin{bmatrix} (Y_{21}+Y_{11}) & (1-Z_sY_{21}) \\ -Y_{21} & Z_sY_{21} \end{bmatrix}}_{\text{Noise Matrices}} \cdot \begin{bmatrix} (v_1+v_s) \\ -i_1 \end{bmatrix} + \begin{bmatrix} -1 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} Y_P v_P \\ i_G \\ i_D \end{bmatrix}. \tag{4}$$

Having derived both the signal and the noise currents, we are now in a position to determine the gain, the

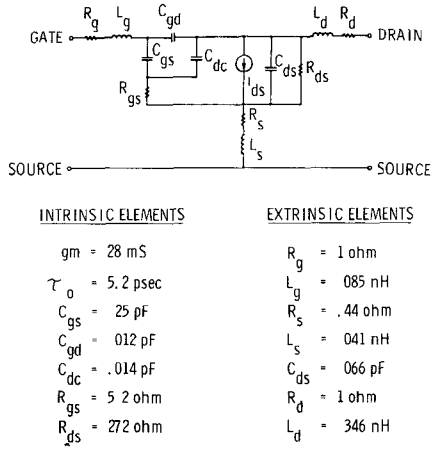


Fig. 4. Equivalent circuit of the MESFET and its elements.

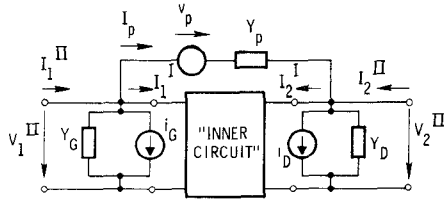


Fig. 5. The common-gate input stage of Fig. 1 and its "outer circuit" noise sources.

reflection coefficients, and the noise figure. Driven by the complex source impedance Z_1 and terminated by the complex load impedance Z_2, the input reflection coefficients $|S_{11}|$ and $|S_{22}|$, as well as the transducer gain G_T of the common gate input stage, are

$$|S_{11}| = \left| \frac{1 - Z_1 Y_{11}^{II} + Z_2 Y_{22}^{II} - Z_1 Z_2 \left(Y_{11}^{II} Y_{22}^{II} - Y_{12}^{II} Y_{21}^{II} \right)}{1 + Z_1 Y_{11}^{II} + Z_2 Y_{22}^{II} + Z_1 Z_2 \left(Y_{11}^{II} Y_{22}^{II} - Y_{12}^{II} Y_{21}^{II} \right)} \right| \tag{5a}$$

$$|S_{22}| = \left| \frac{1 + Z_1 Y_{11}^{II} - Z_2 Y_{22}^{II} - Z_1 Z_2 \left(Y_{11}^{II} Y_{22}^{II} - Y_{12}^{II} Y_{21}^{II} \right)}{1 + Z_1 Y_{11}^{II} + Z_2 Y_{22}^{II} + Z_1 Z_2 \left(Y_{11}^{II} Y_{22}^{II} - Y_{12}^{II} Y_{21}^{II} \right)} \right| \tag{5b}$$

$$G_T = \left(Z_1 + Z_1^* \right) \left(Z_2 + Z_2^* \right) \cdot \left| \frac{Y_{21}^{II}}{1 + Z_1 Y_{11}^{II} + Z_2 Y_{22}^{II} + Z_1 Z_2 \left(Y_{11}^{II} Y_{22}^{II} - Y_{12}^{II} Y_{21}^{II} \right)} \right|^2 \tag{5c}$$

and in accordance with the signal matrix of (4)

$$Y_{11}^{II} = Y_{11}^{I} + Y_G + Y_P \tag{5d}$$

$$Y_{12}^{II} = Y_{12}^{I} - Y_P \tag{5e}$$

$$Y_{21}^{II} = Y_{21}^{I} - Y_P \tag{5f}$$

$$Y_{22}^{II} = Y_{22}^{I} + Y_D + Y_P. \tag{5g}$$

The exact formulas of the inner circuit's admittance parameters Y_{ij}^{I} are given in (1). However, the approximations of (3) may be used as long as the condition (2) is satisfied. At low frequencies, where $Y_{11} \cong Y_{12} \cong 0, Y_{21} \cong g_m$ (transconductance) and $Y_{22} \cong G_{ds}$ (drain–source conductance), the Y_{ij}^{I}-parameters become independent of the series impedance Z_s. Here, as will be shown later, Z_s looses its influence on both gain and optimum noise figure.

B. The Equivalent Noise Parameters

1) The Inner Circuit: We will now focus our attention on the derivation of the circuit's noise parameters. As indicated earlier, this may be accomplished in two steps. Beginning with the inner circuit of Fig. 1 represented by the equivalent circuit of Fig. 3, we transform all sources of noise to the input of our network rendering it noiseless, i.e., $T = 0°\text{K}$. (Fig. 2(d)). This is done by converting the noise matrix of (1) into the noise quantities v_1^{I} and i_1^{I}, external to our circuit

$$v_1^{I} = \frac{-Y_{21}}{(Y_{21} + Y_{22}) + Z_s (Y_{11} Y_{22} - Y_{12} Y_{21})} \cdot \left[(v_1 + v_s) - Z_s i_1 \right] \tag{6a}$$

$$i_1^{I} = \frac{1}{(Y_{21} + Y_{22}) + Z_s (Y_{11} Y_{22} - Y_{12} Y_{21})} \cdot \left[(Y_{11} Y_{22} - Y_{21} Y_{12})(v_1 + v_s) - (Y_{21} + Y_{22}) i_1 \right]. \tag{6b}$$

Taking into account the correlation that exists between the voltage and the current, which is expressed by [4]

$$i_1^{I} = i_n^{I} + Y_{cor}^{I} v_1^{I} \tag{7}$$

we arrive at the equivalent noise parameters of the subcircuit (Fig. 2(d))

$$R_n^{I} = \frac{\overline{|v_1^{I}|^2}}{4kT_0 \Delta f} = \frac{|Y_{21}|^2}{|(Y_{21} + Y_{22}) + Z_s (Y_{11} Y_{22} - Y_{12} Y_{21})|^2} \cdot \left[|1 + Z_s Y_{cor}|^2 R_n + R_s + |Z_s|^2 G_n \right] \tag{8a}$$

$$G_n^{I} = \frac{\overline{|i_n^{I}|^2}}{4kT_0 \Delta f} = \frac{1}{|1 + Z_s Y_{cor}|^2 R_n + R_s + |Z_s|^2 G_n} \cdot \left[R_n G_n + R_s \left(G_n + |Y_{cor}|^2 R_n \right) \right] \tag{8b}$$

$$Y_{cor}^{I} = \frac{\overline{i_1^{I} (v_1^{I})^*}}{\overline{|v_1^{I}|^2}} = \frac{1}{|1 + Z_s Y_{cor}|^2 R_n + R_s + |Z_s|^2 G_n} \cdot \left[Y_{cor}^{I} (Z_s = 0) \left[1 + Z_s^* Y_{cor}^* \right] R_n - \frac{Y_{11} Y_{22} - Y_{12} Y_{21}}{Y_{21}} R_s + Z_s^* \frac{Y_{21} + Y_{22}}{Y_{21}} G_n \right] \tag{8c}$$

$$Y_{cor}^{I} (Z_s = 0) = Y_{cor} \frac{Y_{21} + Y_{22}}{Y_{21}} - \frac{Y_{11} Y_{22} - Y_{12} Y_{21}}{Y_{21}} \tag{8d}$$

$$Z_s = R_s + jX_s. \tag{8e}$$

Unfortunately, the results are rather complex and an at-

tempt to simplify the above formulas seems to be in order. Assuming the use of the device characterized in Fig. 4 and employing resistive series feedback ($Z_s = R_s$), we have studied the limits of frequency and feedback resistance within which certain terms of our formulas become negligible. The results of this investigation are reflected in the following limits and approximation formulas. For

$$Z_s = R_s \leqslant 10\ \Omega \tag{9a}$$

and

$$f \leqslant 10\ \text{GHz} \tag{9b}$$

$$R_n^{\mathrm{I}} \cong \left| \frac{Y_{21}}{Y_{21}+Y_{22}} \right|^2 (R_n + R_s) \tag{10a}$$

$$G_n^{\mathrm{I}} \cong G_n + |Y_{\mathrm{cor}}|^2 \frac{R_n R_s}{R_n + R_s} \tag{10b}$$

$$Y_{\mathrm{cor}}^{\mathrm{I}} \cong \frac{1}{R_n + R_s} \left[Y_{\mathrm{cor}}^{\mathrm{I}}(Z_s = 0)\left[1 + R_s Y_{\mathrm{cor}}^*\right] R_n - \frac{Y_{11}Y_{22} - Y_{12}Y_{21}}{Y_{21}} R_s + R_s \frac{Y_{21}+Y_{22}}{Y_{21}} G_n \right]. \tag{10c}$$

While the formulas for R_n^{I} and G_n^{I} have been considerably reduced, that for $Y_{\mathrm{cor}}^{\mathrm{I}}$ remains rather complicated. Unfortunately, none of the three terms in (8c) is small compared to the others, and further reduction results in errors for $Y_{\mathrm{cor}}^{\mathrm{I}}$ and, consequently, in erroneous noise figures.

The noise figure of our circuit may now be obtained with [5]

$$F^{\mathrm{I}} = F_{\min}^{\mathrm{I}} + \frac{R_n^{\mathrm{I}}}{G_s} \left| Y_s - Y_{s\min}^{\mathrm{I}} \right|^2 \tag{11}$$

where

$$Y_s = G_s + jB_s \tag{11a}$$

is the source admittance,

$$Y_{\mathrm{cor}}^{\mathrm{I}} = G_{\mathrm{cor}}^{\mathrm{I}} + jB_{\mathrm{cor}}^{\mathrm{I}} \tag{11b}$$

is the correlation admittance, and

$$Y_{s\min}^{\mathrm{I}} = G_{s\min}^{\mathrm{I}} + jB_{s\min}^{\mathrm{I}} = \sqrt{\frac{G_n^{\mathrm{I}}}{R_n^{\mathrm{I}}} + \left(G_{\mathrm{cor}}^{\mathrm{I}}\right)^2} - jB_{\mathrm{cor}}^{\mathrm{I}} \tag{11c}$$

is the source admittance for the minimum noise figure

$$F_{\min}^{\mathrm{I}} = 1 + 2R_n^{\mathrm{I}}\left(G_{\mathrm{cor}}^{\mathrm{I}} + G_{s\min}^{\mathrm{I}}\right). \tag{11d}$$

Based on the approximation formulas (10), the deviation of the minimum noise figure from its exact value does not exceed $\Delta F_{\min}^{\mathrm{I}} = 0.3$ dB for $f \leqslant 10$ GHz and $R_s \leqslant 15\ \Omega$ when the device of Fig. 4 is used. However, reasonable accuracy for the optimum source admittance (11c) can only be obtained within the limits of (9). Curves of the exact optimum noise figure as computed with (8) and (11d) are plotted in Fig. 6(a) between 2 GHz and 18 GHz for different series resistance values. The corresponding small-signal gain (5c) is shown in Fig. 6(b), clearly demonstrating the gain leveling capabilities of R_s.

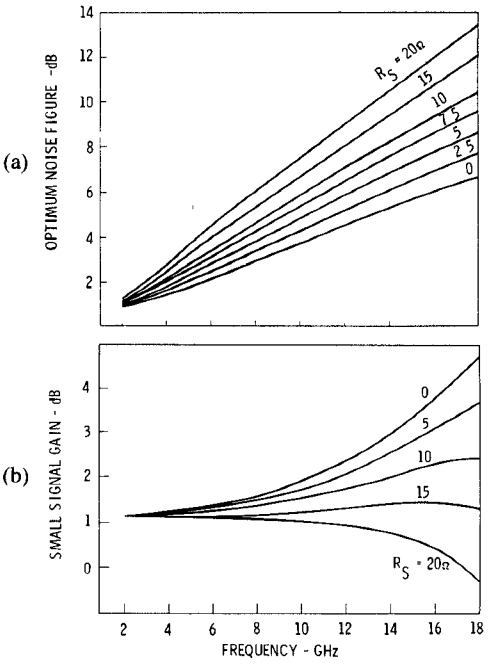


Fig. 6. (a) Noise figure and (b) insertion gain of the common-gate input stage in accordance with Fig. 3.

2) The Common-Gate Input Stage: Rather than repeating the above steps with the entire circuit's noise matrices expressed by (4), we resort to already published results for the remaining transformation [6]. Since [6] also offers a more complete treatment of a typical noise problem, the interested reader might find its study helpful in the understanding of the more condensed procedure given here. With the equivalent noise parameters of the subcircuit (Fig. 2(d)) already known (8), we obtain those of the input stage shown in Fig. 1 by using the formulas published in [6]. They are

$$R_n^{\mathrm{II}} = \frac{1}{|Y_{21}^{\mathrm{I}} - Y_P|^2} \left[|Y_{21}^{\mathrm{I}}|^2 R_n^{\mathrm{I}} + |Y_P|^2 R_P + G_D \right] \tag{12a}$$

$$G_n^{\mathrm{II}} = G_n^{\mathrm{I}} + G_G + |Y_{21}^{\mathrm{I}} + Y_{11}^{\mathrm{I}} - Y_{\mathrm{cor}}^{\mathrm{I}}|^2 \frac{|Y_P|^2 R_P R_n^{\mathrm{I}}}{|Y_{21}^{\mathrm{I}}|^2 R_n^{\mathrm{I}} + |Y_P|^2 R_P + G_D} + \frac{|Y_{11}^{\mathrm{I}} - Y_{\mathrm{cor}}^{\mathrm{I}}|^2 R_n^{\mathrm{I}} + |Y_P|^2 R_P}{|Y_{21}^{\mathrm{I}}|^2 R_n^{\mathrm{I}} + |Y_P|^2 R_P + G_D} G_D \tag{12b}$$

$$Y_{\mathrm{cor}}^{\mathrm{II}} = Y_{\mathrm{cor}}^{\mathrm{I}} + Y_G + \left(Y_{21}^{\mathrm{I}} + Y_{11}^{\mathrm{I}} - Y_{\mathrm{cor}}^{\mathrm{I}}\right) \frac{\left(Y_{21}^{\mathrm{I}}\right)^* Y_P R_n^{\mathrm{I}} + |Y_P|^2 R_P}{|Y_{21}^{\mathrm{I}}|^2 R_n^{\mathrm{I}} + |Y_P|^2 R_P + G_D} + \left(Y_{11}^{\mathrm{I}} + Y_P - Y_{\mathrm{cor}}^{\mathrm{I}}\right) \frac{G_D}{|Y_{21}^{\mathrm{I}}|^2 R_n^{\mathrm{I}} + |Y_P|^2 R_P + G_D}. \tag{12c}$$

As in the case of the noise parameters of the inner circuit (8), we are confronted with a complicated set of formulas (12) if we insist on an exact solution. Again, an effort to simplify the expressions we arrived at is warranted. When using the device of Fig. 4, we find that in most practical cases the third term of the noise conductance G_n^{II} is small compared to the other three terms. If, in addition, we choose $G_D = 0$ as we have done in the input network of Fig. 10, our set of formulas (12) experiences significant

reductions

$$R_n^{II} \cong \frac{1}{|Y_{21}^I - Y_P|^2}\left[|Y_{21}^I|^2 R_n^I + |Y_P|^2 R_P\right] \tag{13a}$$

$$G_n^{II} \cong G_n^I + G_G \tag{13b}$$

$$Y_{cor}^{II} \cong Y_{cor}^I + Y_G + \left(Y_{21}^I + Y_{11}^I - Y_{cor}^I\right)\frac{\left(Y_{21}^I\right)^* Y_P R_n^I + |Y_P|^2 R_P}{|Y_{21}^I|^2 R_n^I + |Y_P|^2 R_P}. \tag{13c}$$

As can be seen from (13b), the effect of parallel feedback on the input stage's noise conductance in the absence of G_D is, as expected, negligible. However, in case of $G_D \neq 0$, the influence of the output conductance G_D on the circuit's noise parameters (12) can no longer be ignored.

In the foregoing, we have assembled the parameters that enable us to calculate the gain, the reflection coefficients, the optimum noise figure, and the noise figure of the common-gate input stage. In the following, we will briefly examine the influence of the individual circuit parameters on these quantities.

III. Computed Performance Results

Before we focus our attention on the characteristics of a practical amplifier design, it seems appropriate to examine briefly the accuracy of our approximation formulas for the Y-parameters (3) and the noise parameters (10) and (13). However, rather than comparing the exact and approximated values of Y_{ij}^{II}, R_n^{II}, G_n^{II}, and Y_{cor}^{II}, we will compare those of the gain G_T (5c), the minimum noise figure F_{min}^{II} (11d), and the optimum source admittance $Y_{s\,min}^{II}$ (11c) as computed by means of the exact ((1), (8), (12)) and the approximated values ((3), (10), (13)) of the Y-parameters and the noise parameters. Two common-gate input circuits that are similar to the 2–12-GHz and 2–18-GHz input stages shown as part of the two-stage amplifier designs in Fig. 10 serve as the study vehicles. The schematic and the elements of the circuits are presented in Fig. 7 and vary from those of Fig. 10 only by the series feedback resistors $R_s = 10\ \Omega$ that have been inserted to test the accuracy of our approximation formulas in the presence of series feedback. When comparing the results shown in Figs. 8 and 9, we find excellent agreement for the minimum noise figures F_{min}^{II} at frequencies of $f \leqslant 14$ GHz, as well as for the optimum source impedances $Y_{s\,min}^{II}$ at frequencies of $f \leqslant 10$ GHz in the case of both circuits. The latter is important when using the approximation formulas (10) and (13) in order to calculate the noise figure (11).

As explained earlier, the values of the elements surrounding the transistor in Fig. 1 were chosen for a desired gain curve and stable operation of the amplifier. Such measures, when applied over wide bandwidths, result in fairly low gains and sometimes even loss at the low end of the frequency band. For this reason, and the fact that the gain of the common-gate input stage depends heavily on the load presented to it by the following amplifier stage, it is almost pointless to study the common-gate input stage

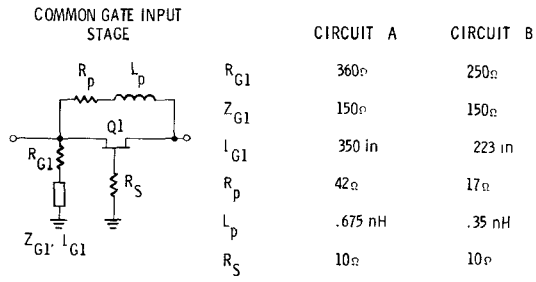


Fig. 7. Common-gate input stages using series feedback.

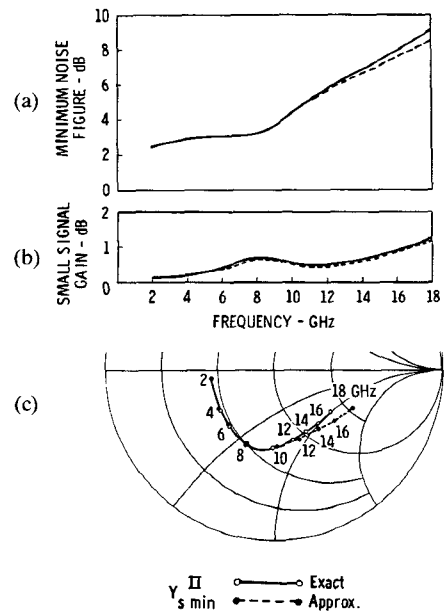


Fig. 8. Comparison of exact (solid curves) and approximated (dashed curves) performance parameters of circuit "A" in Fig. 7.

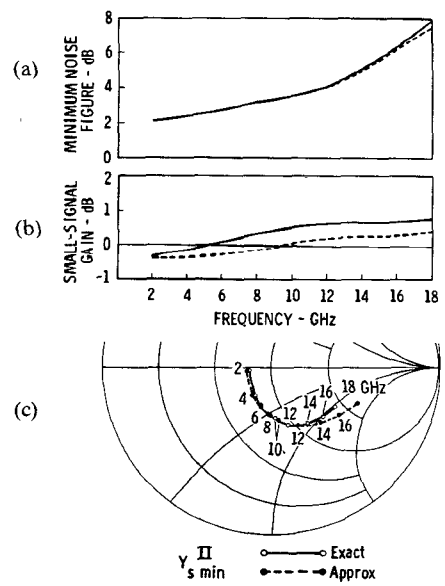
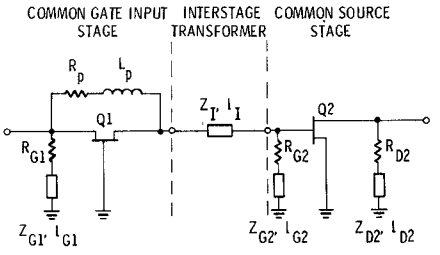


Fig. 9. Comparison of exact (solid curves) and approximated (dashed curves) performance parameters of circuit "B" in Fig. 7.



FREQUENCY BAND	2-12 GHz	2-18 GHz
R_{G1}	360Ω	250Ω
Z_{G1}	150Ω	150Ω
l_{G1}	350 in	.223 in
R_p	42Ω	17Ω
L_p	.675 nH	35 nH
Z_I	150Ω	150Ω
l_I	.129 in	.064 in
R_{G2}	170Ω	300Ω
Z_{G2}	150Ω	150Ω
l_{G2}	214 in	193 in
R_{D2}	320Ω	260Ω
Z_{D2}	125Ω	135Ω
l_{D2}	.051 in	.083 in

Fig. 10. Simple two-stage amplifier with common-gate input stage.

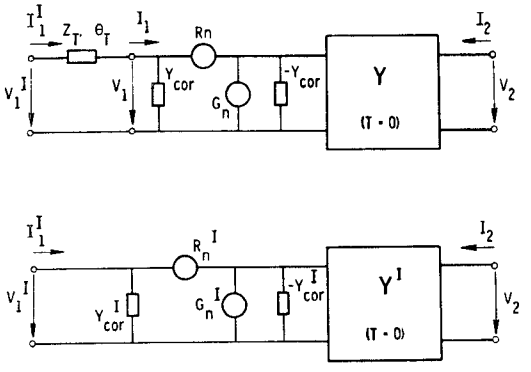


Fig. 11. Noise transformation in a lossless transmission line.

between 50-Ω terminations. Therefore, we extend our analysis to an amplifier module consisting of the common-gate input stage followed by a common-source second stage in accordance with the simple network of Fig. 10. Both active devices in the schematic of Fig. 10 ($Q1$ and $Q2$) are identical and characterized by the equivalent circuit of Fig. 4. The interstage transformer improves the matching between the two active circuits. However, it also transforms the noise parameters even though the optimum noise figure of such a transformation remains unaltered as long as the transmission-line element is lossless. For reasons of completeness, we present the transformed noise parameters (A1), which are based on the network of Fig. 11 in Appendix I. After obtaining the noise parameters of the common-gate input stage with (8) and (10) or, since in our case $Z_s = 0$, with (A2) of Appendix II and those of the common-source stage with the formulas of [6], we finally need to cascade these noisy two-ports and the interstage

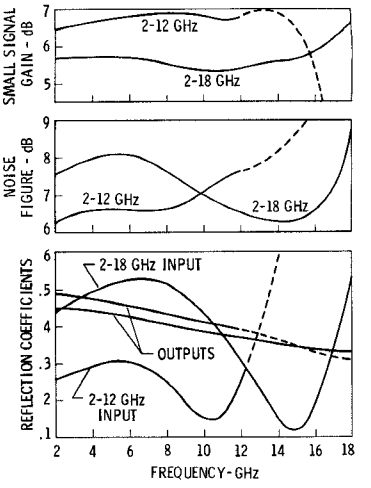


Fig. 12. Performance of the two-stage amplifiers of Fig. 10.

transformer (A1) between them to arrive at the overall noise figure. This can be done with the formulas reported in the literature [7].

It should be pointed out that the circuit of Fig. 10 does not make use of series feedback ($Z_s = 0$). Its elimination became necessary, for the real component of Z_s (i.e., R_s) has a strong influence on the amplifier's optimum noise figure. This is clearly demonstrated in the curves of Fig. 6(a), which show the common-gate input stage's optimum noise figure for the simple circuit of Fig. 2(c) when $Z_s = R_s$ and the device of Fig. 4 is used. If, therefore, the amplifier's noise figure is of concern, it is advisable to choose $Z_s = 0$ provided that stable operation can be maintained with the remaining circuit elements. The series resistance's tilting effect on gain is illustrated in the curves of Fig. 6(b). Here, we chose to plot the transducer gain rather than the maximum available gain because the circuit is either conditionally stable or unstable in the band of interest if $0 \leqslant R_s \leqslant 20\ \Omega$.

The optimized circuit elements of the two-stage amplifier whose values are supplied in Fig. 10 present a compromise between gain, noise figure, and VSWR performance, which are plotted in Fig. 12 for the 2–12-GHz and the 2–18-GHz frequency band. The curves clearly demonstrate that of the four parameters shown, the input match is the most difficult one to obtain over a frequency range in excess of 3 octaves while simultaneously maintaining acceptable gain and noise figure performance. When comparing the input reflection coefficients of the 2–12-GHz and the 2–18-GHz amplifiers, we learn that only the former exhibits an acceptable performance, for the input VSWR of the 2–18-GHz design approaches 3.3:1. While the gain and the noise figure of the latter show respectable results, its overall performance is impaired by the relatively high input reflection coefficient. Generally, it has been found, however, that a common-gate input stage is capable of improving the input match of a 2–18-GHz feedback or lossy match amplifier. [8]. On the other hand, this improvement does not match the input VSWR performance achievable with a distributed amplifier employing devices similar to those characterized by the equivalent circuit of Fig. 4. [8]

IV. Conclusion

The design of a common-gate input stage requires much more attention to the MESFET parameters than does the common-source input stage employing the same device. Especially, the elimination of stability problems and negative output impedances at high frequencies are dominating the design procedure. As shown, this task can be accomplished with relatively simple circuits that make use of lossy shunts and lossy feedback. However, as demonstrated, the lossy circuit elements have a significant impact on gain and noise figure. Therefore, formulas for the admittance and noise parameters have been developed that allow one to calculate the gain and noise figure of the common-gate input stage. A study of the theoretical results shows the degree of the series feedback's negative influence on noise figure. Its effect at high frequencies is significant; thus, resistive series feedback should be avoided whenever low noise figures are of primary concern. However, its ability to tilt the gain curve may be desirable in case a flat gain performance is demanded of the common-gate input circuit. Since the gain of a common-gate input stage stabilized by resistive circuitry is relatively low, accurate noise-figure calculations require the inclusion of at least the following stage into the computations. Hence, the performances of two relatively simple common-gate common-source circuits have been studied over the 2–12-GHz and 2–18-GHz frequency bands. Only the 2–12-GHz band unit exhibits an acceptable input match, indicating that more complicated networks are needed to cover the 2–18-GHz band [8].

Appendix I
Noise Transformation in a Transmission Line

A noisy two-port characterized by its equivalent noise parameters R_n, G_n, and Y_{cor} is preceded by a lossless transmission line of the characteristic impedance Z_T and electrical length θ_T as shown in Fig. 11(a). Incorporation of the transmission line into the new two-port of Fig. 11(b) leads to the new set of noise parameters

$$R_n^{\mathrm{I}} = R_n\left[\cos^2\theta_T + |Z_T Y_{s\min}|^2 \sin^2\theta_T - B_{cor} Z_T \sin 2\theta_T\right] \tag{A1a}$$

$$G_n^{\mathrm{I}} = \frac{R_n}{R_n^{\mathrm{I}}} G_n \tag{A1b}$$

$$G_{cor}^{\mathrm{I}} = \frac{R_n}{R_n^{\mathrm{I}}} G_{cor} \tag{A1c}$$

$$B_{cor}^{\mathrm{I}} = \frac{R_n}{R_n^{\mathrm{I}}}\left[B_{cor}\cos 2\theta_T + \left(\frac{1-|Y_{s\min}Z_T|^2}{2Z_T}\right)\sin 2\theta_T\right] \tag{A1d}$$

$$Y_{s\min} = G_{s\min} - jB_{cor} \tag{A1e}$$

$$G_{s\min} = \sqrt{\frac{G_n}{R_n} + (G_{cor})^2}\,. \tag{A1f}$$

Appendix II
Noise Parameters of the Common-Gate Input Stage for $Z_s = 0$

The Y-parameters (1) and the noise parameters of the inner circuit of Fig. 1 (8) take on a much simpler form for the case of $Z_s = 0$. Substituting (8) into (12) for $Z_s = 0$ yields the noise parameters of the common-gate input stage

$$R_n^{\mathrm{II}} = \frac{1}{|Y_{21}+Y_{22}+Y_P|^2}\left[|Y_{21}|^2 R_n + |Y_P|^2 R_P + G_D\right] \tag{A2a}$$

$$G_n^{\mathrm{II}} = G_G + G_n + |Y_{11}-Y_{cor}|^2 \frac{|Y_P|^2 R_P R_n}{|Y_{21}|^2 R_n + |Y_P|^2 R_P + G_D} + \frac{|Y_{11}+Y_{21}-Y_{cor}|^2 R_n + |Y_P|^2 R_P}{|Y_{21}|^2 R_n + |Y_P|^2 R_P + G_D} G_D \tag{A2b}$$

$$Y_{cor}^{\mathrm{II}} = Y_G + Y_{11} + Y_{12} + (Y_{21}+Y_{22}+Y_P) \cdot \frac{G_D - Y_{21}^*(Y_{11}-Y_{cor})R_n}{|Y_{21}|^2 R_n + |Y_P|^2 R_P + G_D}. \tag{A2c}$$

In many practical cases

$$|Y_{21}+Y_{11}-Y_{cor}|^2 \gg |Y_{11}-Y_{cor}|^2 \tag{A3}$$

and, indeed, very accurate noise conductances G_n^{II} can be obtained when the third term of (A2b) has been dropped. This fact emphasizes, in contrast to common-source networks [6], the considerable influence of G_D on the noise figure when employing common-gate circuits.

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